CLAIMS

What is claimed is:

1. A method of operating an integrated circuit device, the method comprising the acts of:

programming a first memory cell associated with a first digit line to a first data value;

programming a second memory cell associated with a second digit line to a second data value, the second data value being complementary with respect to the first data value;

firing a first sense amplifier associated with the first digit line;

firing a second sense amplifier associated with the second digit line after a time delay with respect to the act of firing the first sense amplifier associated with the first digit line;

detecting a measured data value associated with the second digit line; and

comparing the measured data value to the second data value to determine whether the first digit line is short circuited to the second digit line.

2. The method set forth in claim 1, comprising the act of selecting the sense amplifier associated with the first digit line and the sense amplifier associated with the second digit line such that the first digit line and the second digit line are adjacent to each other on the die of an integrated circuit device.

3. The method set forth in claim 1, comprising the act of programming a time value for the time delay.

4. The method set forth in claim 1, wherein the time delay is in the range of 2 to15 nanoseconds.

5. The method set forth in claim 1, comprising the act of placing the integrated circuit device in a test mode.

6. The method set forth in claim 1, comprising the act of repairing a short circuit between the first digit line and the second digit line.

7. An integrated circuit device, comprising:

a first sense amplifier that is associated with a first digit line;

a second sense amplifier that is associated with a second digit line; and

a circuit that adds a time delay between a firing operation of the second sense amplifier with respect to a firing operation of the first sense amplifier to allow detection of whether a short circuit exists between the first digit line and the second digit line.

8. The integrated circuit device set forth in claim 7, wherein the first digit line and the second digit line are adjacent to each other.

9. The integrated circuit device set forth in claim 7, wherein the time delay is in the range of 2 to 15 nanoseconds.

10. The integrated circuit device set forth in claim 7, wherein the first sense amplifier comprises a portion of a first bank of sense amplifiers and the second sense amplifier comprises a portion of a second bank of sense amplifiers.

11. The integrated circuit device set forth in claim 7, wherein the circuit that adds the time delay operates in a test mode of the integrated circuit device.

12. The integrated circuit device set forth in claim 7, wherein the integrated circuit device comprises a dynamic random access memory ("DRAM") device.

13. The integrated circuit device set forth in claim 7, wherein the integrated circuit device comprises a microprocessor.

14. An integrated circuit device, comprising:

a first sense amplifier that is associated with a first digit line;

a second sense amplifier that is associated with a second digit line; and

means for adding a time delay between a firing operation of the second sense amplifier with respect to a firing operation of the first sense amplifier to allow detection of whether a short circuit exists between the first digit line and the second digit line.

15. The integrated circuit device set forth in claim 14, wherein the first digit line and the second digit line are adjacent to each other.

16. The integrated circuit device set forth in claim 14, wherein the time delay is in the range of 2 to 15 nanoseconds.

17. The integrated circuit device set forth in claim 14, wherein the first sense amplifier comprises a portion of a first bank of sense amplifiers and the second sense amplifier comprises a portion of a second bank of sense amplifiers.

18. The integrated circuit device set forth in claim 14, wherein the means for adding a time delay operates in a test mode of the integrated circuit device.

19. The integrated circuit device set forth in claim 14, wherein the integrated circuit device comprises a dynamic random access memory ("DRAM") device.

20. The integrated circuit device set forth in claim 14, wherein the integrated circuit device comprises a microprocessor.

21. An electronic device, comprising:

a processor adapted to execute instructions;

a storage device adapted to store instructions to be executed by the processor; and

a memory device that receives information stored on the storage device, the memory device comprising:

a first sense amplifier that is associated with a first digit line;

a second sense amplifier that is associated with a second digit line; and

a circuit that adds a time delay between a firing operation of the second sense amplifier with respect to a firing operation of the first sense amplifier to allow detection of whether a short circuit exists between the first digit line and the second digit line.

22. The electronic device set forth in claim 21, wherein the first digit line and the second digit line are adjacent to each other.

23. The electronic device set forth in claim 21, wherein the time delay is in the range of 2 to 15 nanoseconds.

24. The electronic device set forth in claim 21, wherein the first sense amplifier comprises a portion of a first bank of sense amplifiers and the second sense amplifier comprises a portion of a second bank of sense amplifiers.

25. The electronic device set forth in claim 21, wherein the circuit that adds the time delay operates in a test mode of the integrated circuit device.

26. The electronic device set forth in claim 21, wherein the electronic device comprises a computer system.